REMARKS

While claims 12, 13, 16-19 are indicated to be allowable if properly rewritten, the claims 23-30 are allowed. However, claims 1-11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,345,072 to Liu et al. (Liu) and further in view of U.S. Patent 5,512,898 to Norsworthy et al. (Norsworthy).

Claim 1 calls for an asymmetric digital subscriber loop (ADSL) modem that includes an integrated circuit that may contain an analog-to-digital converter to produce data at a relatively higher data rate. In the integrated circuit, a *device may couple to the analog-to-digital converter to reduce the higher data rate data from the analog-to-digital converter to a lower data rate.* Finally, a multiplexer may *multiplex the lower data rate data and control information and transmit* the data and control information *externally of the integrated circuit.*

In the § 103 rejection of claim 1, the Examiner contends that, Liu reference is directed to xDSL modem configured with the digital and analog sections separated so as to improve noise performance in the analog front-end sections. Furthermore, Liu is asserted to teach that some or all of the functions of DSL Analog Modem circuit 205 may be grouped and implemented in single chip (integrated circuit) form. However, the Examiner is requested to consider the specific claim limitations of the ADSL modem in claim 1 including the device in the integrated circuit that *may couple to the analog-to-digital converter to reduce the higher data rate* and the mutiplexer to *multiplex the lower data rate data and control information and transmit that externally of the integrated circuit.*

Liu does not show the use of a decimation filter in the analog section 205. Moreover, Liu does not disclose a multiplexer in the analog section 205 to multiplex normal data rate and control words. Norsworthy, on the other hand, merely teaches use of a decimation section 306 coupled to an oversampling A/D converter 220' to remove noise beyond the Nyquist frequency and to lower the sampling rate of the Nyquist rate. The Examiner reasons that, as known in the art, decimation is a process of lowering the sampling rate of a signal. Hence, use of a decimation filter is taught or suggested after an A/D converter to lower the data rate of the oversampling A/D converter.

However, absent a specific hint or a suggestion or a reason to modify the teachings of Liu using the Norsworthy teachings or suggestions, regardless of whether the Norsworthy and Liu

references are considered solely or jointly, cannot result in the ADSL modem of claim 1. Accordingly, the Examiner fails to show where Norsworthy teaches an implementation of the claimed device, which somehow is used after the A/D converter 213 of Liu's teachings to lower the data rate, as indicated by the specific claim 1 limitations. The mere fact that a reference can be modified is not sufficient to establish a *prima facie* case of obviousness. M.P.E.P. § 2143.01. Thus, for at least this reason, the Examiner still fails to establish a *prima facie* case of obviousness for independent claim 1. Dependent claims 2-10 are patentable for at least the reason that these claims depend from an allowable claim.

Claim 11 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Liu and further in view of U.S. Patent 6,028,891 to Ribner et al. (Ribner). The Examiner asserts that because Ribner teaches a 512 point FFT 50 and Q.A.M decoder, Ribner teaches that an FFT transformer and a line decoder may be implemented into the second integrated circuit of Liu. However, the Examiner does not point to a specific language in Ribner or Liu teaching the second integrated circuit that includes a fast Fourier transformer and a line decoder.

Instead, when considering the particular limitations of claim 11, the method of claim 11 recites that the second integrated circuit includes a fast Fourier transformer and a line decoder. Therefore, implementation of an FFT transformer and a line decoder as taught by Ribner into the second integrated circuit of Liu would not have been apparent to one of ordinary skill in the art. A *prima facie* case of obviousness of claim 11 is not made out.

Independent claim 14 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Norsworhthy. Norsworhthy is shown to teach serializing the data. However, Norsworhthy neither teaches nor suggests a method that includes decreasing the data rate of analog to digital converted data before serializing the data and transferring to a second integrated circuit device.

The Examiner notes that Norsworthy does not disclose that data is serialized and the coder-decoder is implemented on an integrated circuit. The Examiner is respectfully requested to show where the cited reference teaches or suggests these claim limitations. Absent such showing, it would not be apparent to one skilled in the art that the coder-decoder can be physically separate from the receiver 250, and can be implemented in a single chip (IC) form, rendering obvious the claim 14 limitation that data is processed serially. Therefore, for at the

reasons set forth above, claim 14 and the rejected dependent claims are in condition for allowance. The Examiner is respectfully requested to reconsider all the pending claims.

In view of these remarks, the application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested.

Respectfully submitted,

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Applicants: MICHAEL J. MCTAGUE, ET AL.
Serial No.: 09/471,435
Filing Date: December 23, 1999
Title: ASYMMETRIC DIGITAL SUBSCRIBER LOOP MODEM

1. Reply to Paper No. 10 dated May 20, 2003; and
2. Fax Coversheet.